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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/645,682	08/21/2003	Yi-Nan Chen	10112801	8288

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EXAMINER	
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ART UNIT	PAPER NUMBER
2812	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Claim Objections

Claims 6 and 11 are objected to because of the following informalities: "second liner oxide layer" should be "second liner layer. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-14 are rejected under 35 U.S.C. § 102(e) as being anticipated by Shu 2003/0181016.

Shu discloses a method for filling a uniform mask layer in a trench of a trench capacitor of a DRAM, comprising :

providing a semiconductor substrate 200, wherein a first liner oxide layer 202 and a second liner nitride layer 204 and a mask BSG layer 208 sequentially formed thereon, and the semiconductor substrate has a dense trench area 210 and a less dense trench area 220 with a plurality of trenches formed in both areas

respectively; fig. 2B and para. 23+,

conformably forming a doped insulating layer (216, Arsenic doped glass, ASG) covering the second liner layer 204 and the trenches 212, 214,

forming a photoresist layer 230, 240 covering the doped insulating 216 layer and the trenches are filled with the photoresist layer 230, 240,

etching the photoresist layer 230, 240 at an angle (25-90 degree) until the dense trench area and the less dense trench area in the semiconductor substrate are exposed to leave the photoresist layer in the trenches, fig. 2D-2E, para. 26,

etching the photoresist layers 230', 240' in the trenches, and a uniform thickness of the photoresist layers in each trench is achieved,

etching the doped insulating layer using the photoresist layers as etching masks until the exposed doped insulating layer is removed to leave the doped insulating layer in the trenches; fig. 2F,

removing the photoresist layer, and diffusing the doped insulating layers to form a plurality of doped areas the semiconductor substrate, wherein the doped areas are substantially the same size, para. 29 and fig. 2G.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-14 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-8 of copending Application No. 10/283,977 (Pub. No. US 2003/0181016 A1). Although the conflicting claims are not identical, they are not patentably distinct from each other because the wording of pad layer, shielding layer and higher number of trench etc. are similar to the liner layer, mask layer and dense trench area, respectively.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Any inquiry of a general nature or clerical matters or relating to the status of this application or proceeding should be directed to the Group customer service whose telephone number is (703) 306-3329 and Fax number (703) 872-9306. Group receptionist telephone number 703-308-0956.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to H. Jey Tsai whose telephone number is (703) 308-1374. The examiner can normally be reached on from 7:00 Am to 4:00 Pm., Monday thru Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (703) 308-3325. The fax phone number for this Group is (703) 872-9306.

hjt

12/21/03

H. Jey Tsai
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